"Digital Craftmanship"

DESSERT project

(vhf Data Exchange System tranScEiver pRoTotype in sdr)

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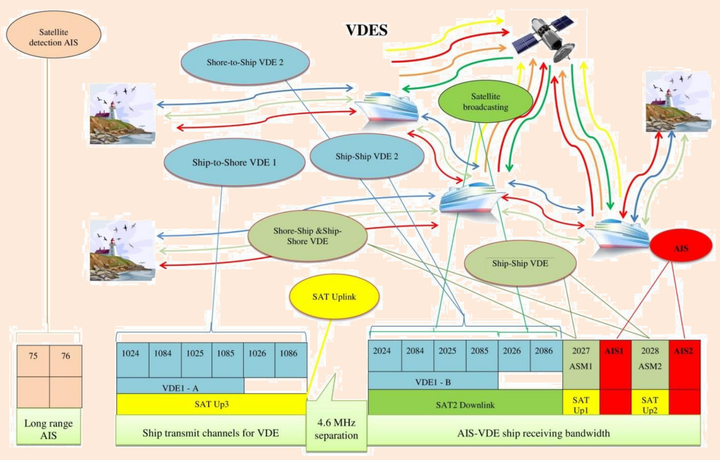
Abstract - DESSERT project aims at designing and implementing two transceiver prototypes of VDES standard, i.e. the brand-new standard for maritime communications. Transceiver prototypes are implemented by exploiting the *SDR technology* and support AIS, ASM and VDE channels, enabling different modulation types and data rates. The prototypes are tested in-lab through on-air transmissions.

VDES Overview

VDES is the next generation standard for digital maritime communications. It integrates three types of data channels, i.e. AIS, ASM (both already operational) and VDE (not yet operational).



VDES Tx modes:

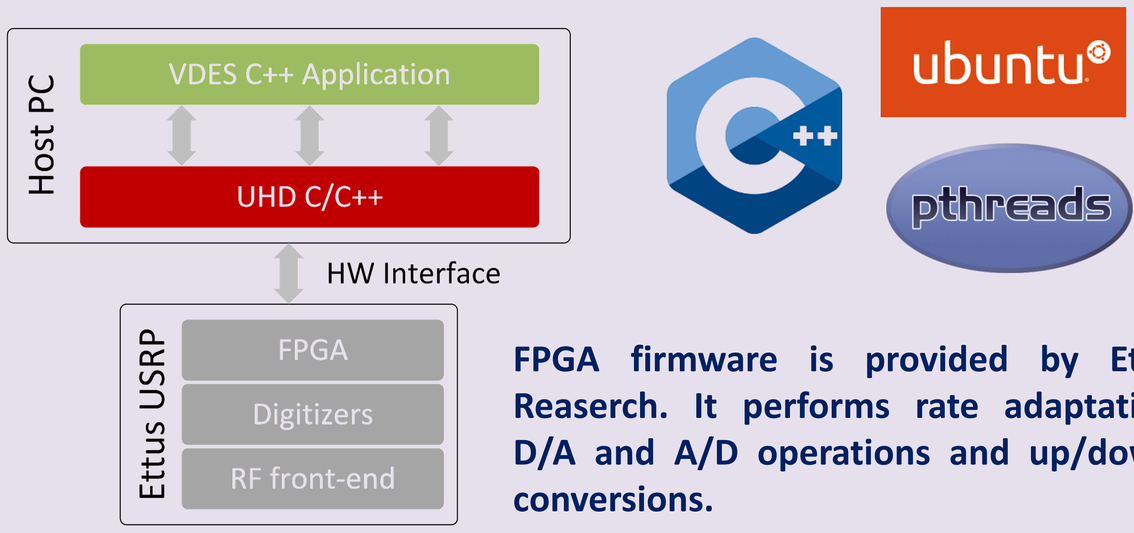
Annex			2 ASM	3 VDE-TER	3 VDE-TER	3 VDE-TER
Channel Bandwidth (kHz)			25	25	50	100
Symbol Rate			9.6	19.2	38.4	76.8
Rolloff factor[2]			0.35	0.3	0.3	0.3
Modulation and coding scheme	**Signal info**	**CQI**	**Total throughput kbit/s**			
MCS-0 (π/4 QPSK, no coding)	0, 0, 0, 0	0	19.2	future	future	future
MCS-1 (π/4 QPSK, CR = 1/2)	0, 0, 0, 1	1	TBD	38.4	76.8	153.6
MCS-3 (8PSK, CR = 3/4)	0, 0, 1, 1	3	Future	57.6	115.2	230.4
MCS-5 (16QAM, CR = 3/4)	0, 1, 0, 1	5	Future	76.8	153.6	307.2

VDES main advantages:

- VDE channels support higher data rate w.r.t. AIS and ASM ones;
- first step to e-Navigation;
- improved global environment and weather knowledge thanks to satellite link;
- new shorter polar routes enabling reduced time and costs.

SW Implementation & HW platform

Designed architecture is then implemented into the C++ multi-threading framework, which communicates with USRP FPGA through Ettus UHD.



FPGA firmware is provided by Ettus Reaserch. It performs rate adaptation, D/A and A/D operations and up/down-conversions.

Transceiver HW platform

- Intel i7-4790K @ 4GHz
- 8 GB DDR3 RAM

- USRP N200
- WBX daughterboard

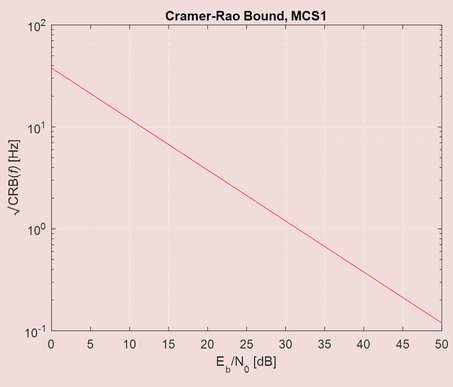
- VHF antenna

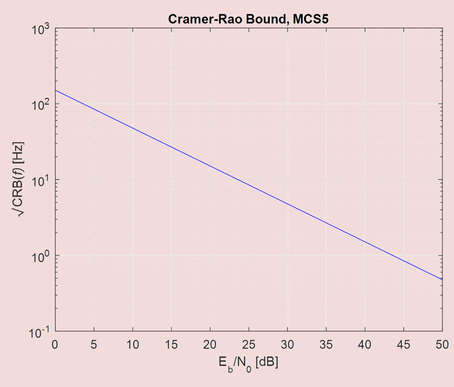
Architecture Design

Main challenges

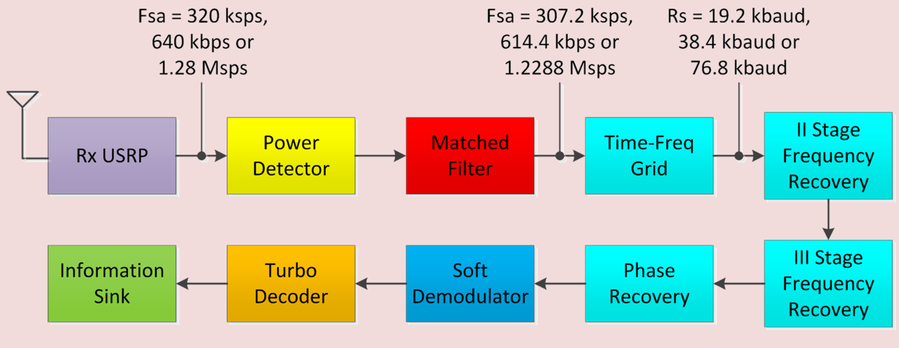
The number of pilot symbols foreseen in the VDES standard is limited. Furthermore, a residual frequency offset of few Hz leads to

$$\Delta_f = 2\pi f_{err} T_{burst} \sim 80^\circ$$ **Detrimental**

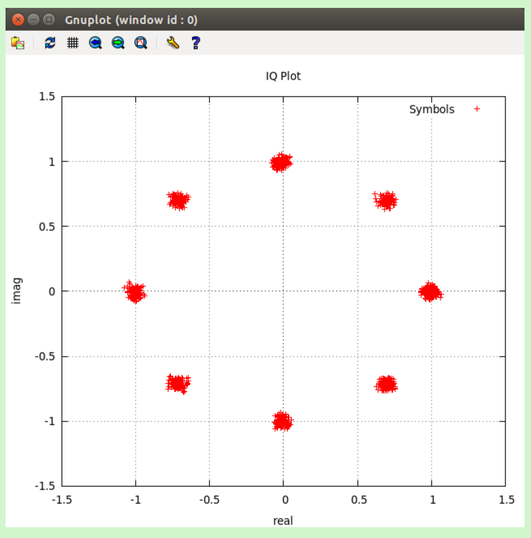


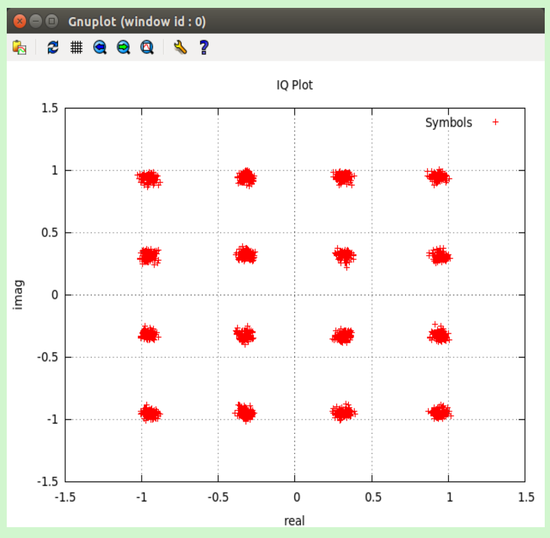


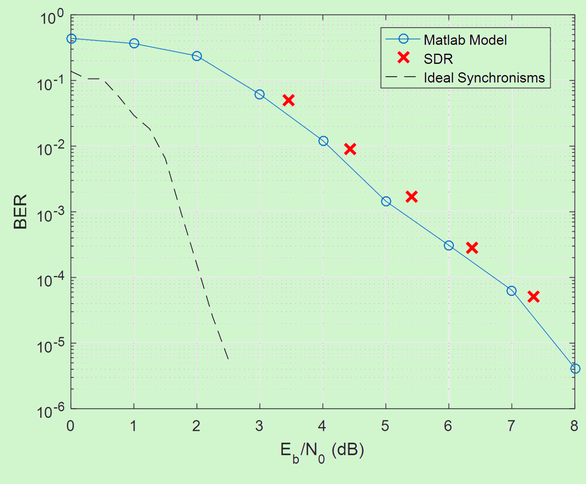
Final Rx Architecture



Summary & Results







- ❑ **MCS1, MCS3, MCS5 supporting different bit-rates implemented and running real-time.**
- ❑ **BER performance measured real-time shows limited detriment w.r.t. Matlab model performance.**
- ❑ **Meaningful data real-time transmission with a carousel mechanism.**